Dynamic Offset-Cancellation Techniques

Kofi Makinwa

Electronic Instrumentation Laboratory, DIMES

Delft University of Technology

Delft, The Netherlands

TU Delft

Delft University of Technology.

Smart Sensor Systems ‘02

Motivation

- Many sensors (e.g. thermopiles, bridges, hall sensors) output DC signals in the millivolt range
- These signals are best processed on-chip
- However, the offset of basic IC amplifiers is **also** in the millivolt range, especially in CMOS
- Therefore, special techniques are required to reduce the offset of IC amplifiers

Outline

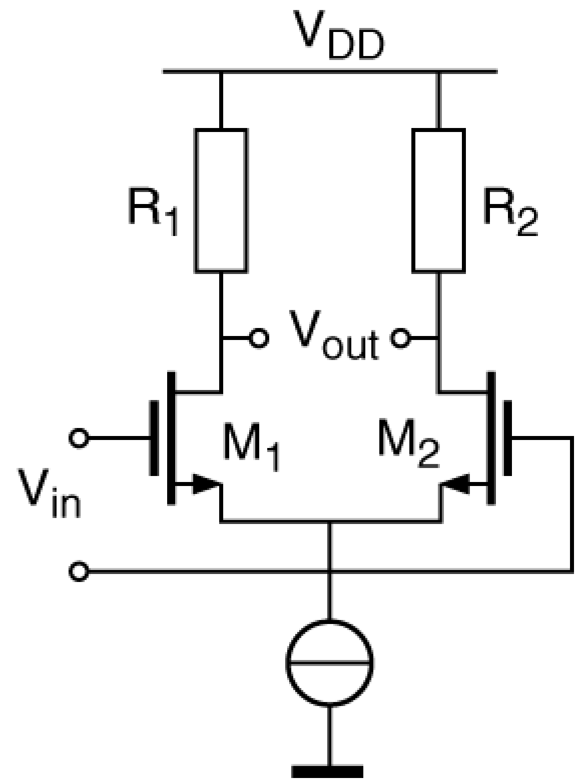
- Differential amplifiers
  - Offset and 1/*f* noise
- Trimming
- Dynamic Offset Cancellation
  - Auto-zeroing
  - Chopping
- Interfacing Examples
- Conclusion
- References

Differential Amplifiers

Differential amplifiers are widely used to amplify DC signals

Balanced structure is

- Nominally offset free
- Rejects common-mode and power supply interference
- Easily realized in both CMOS and bipolar technologies

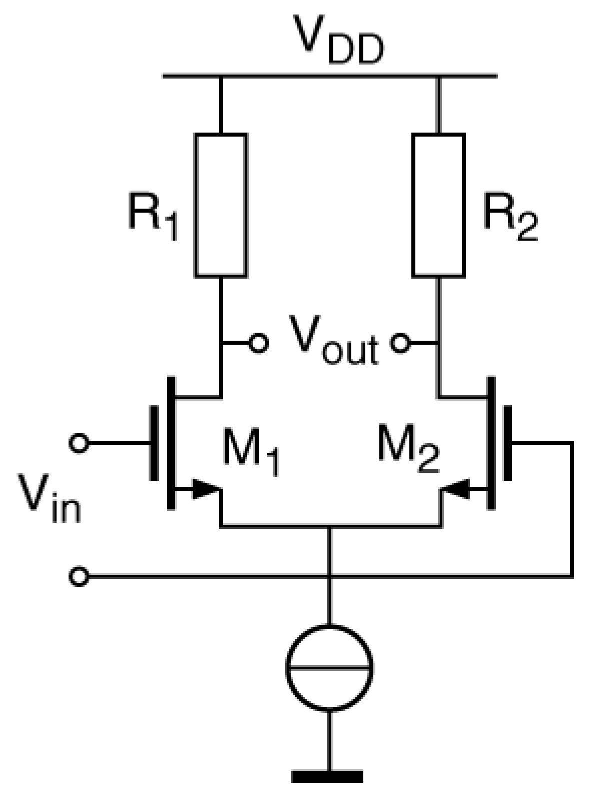


Offset in Differential Amplifiers

Component mismatch ⇒ **offset**
e.g. $R_1 \neq R_2$, $M_1 \neq M_2$

Mismatch is mainly due to
- Process variation
- Lithographic errors

All other things being equal:
Bipolar ⇒ V_{os} ~ 0.1mV
CMOS ⇒ 10 -100 times worse!



Drift and Noise

Drift

- Temperature, ageing and packaging stress cause time-varying offset
- Trimming bipolar DA's reduces **both** offset and temperature drift [1]. Not true of MOSFETs!

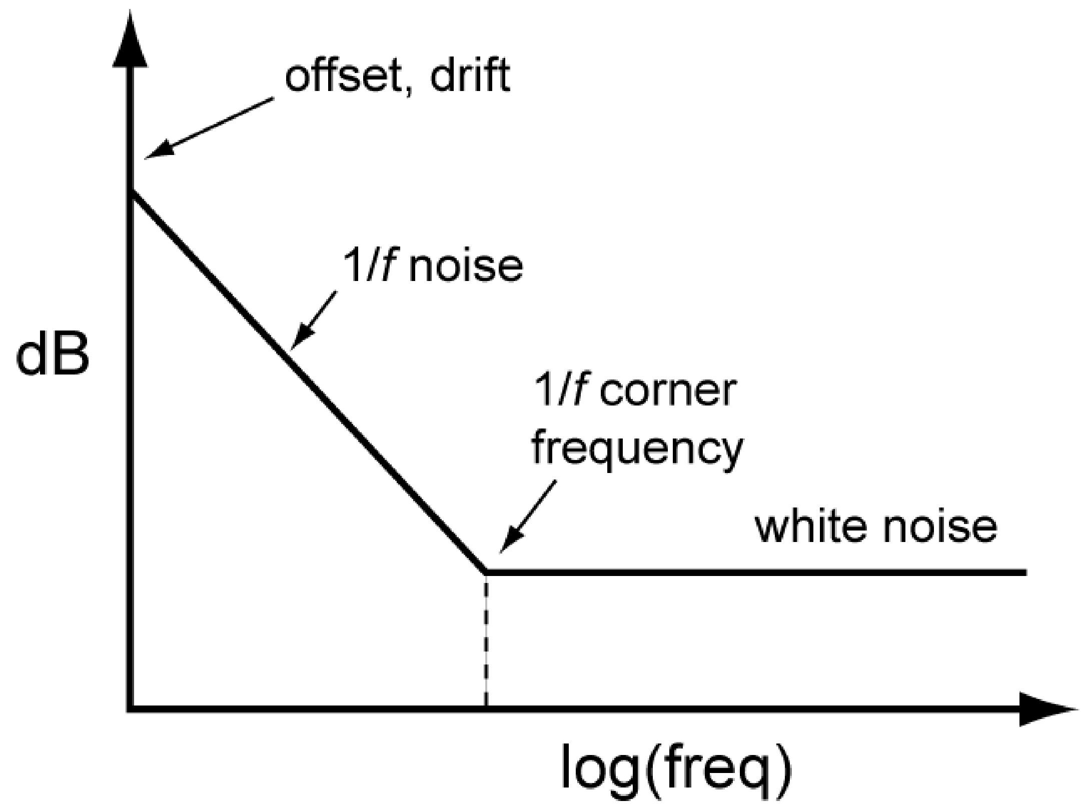
1/*f* (or flicker) noise

- MOSFETs are worse than bipolar transistors
- Varies inversely with transistor area

Amplifier Behaviour Near DC

Characterized by

- Offset
- Drift
- 1/*f* noise
- PSRR, CMRR



What to Do?

Offsets and 1/*f* noise are part of life

But we can reduce offset “enough” by

1. Using “large” devices and good layout [2]
2. Trimming (bipolar) or by
3. Dynamic offset-cancellation (DOC) techniques

DOC techniques also reduce 1/*f* noise!

Trimming

External potentiometers

- Extra component and extra pins

In IC technology [3]

- Laser trimming
- Component switching
  - Zener zapping
  - Fusible links
  - PROM

Trimming $\Rightarrow$ extra test infrastructure

DOC Techniques

Auto-zeroing	Chopping
Sampled data	Continuous time
Sample offset, then subtract	Modulate offset away from DC

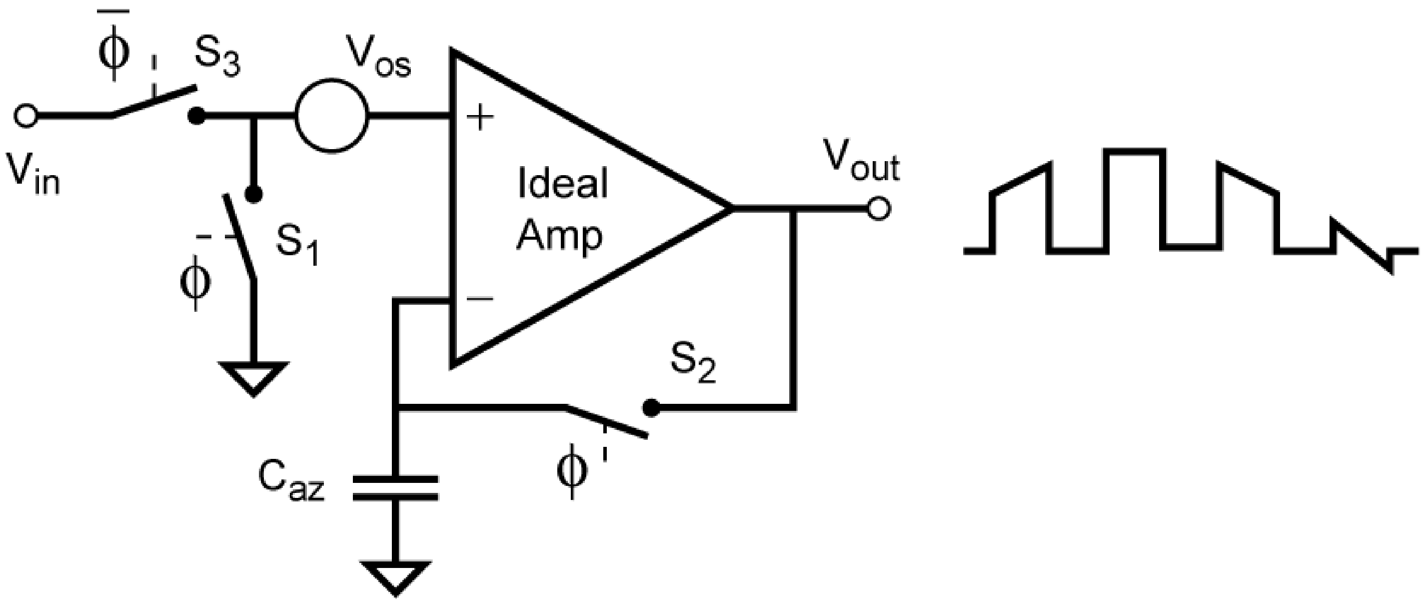
Switches required $\Rightarrow$ CMOS or BiCMOS

DOC Techniques Versus Trimming

+ reduction of offset and 1/*f* noise
+ excellent long term stability
+ no additional costs for testing

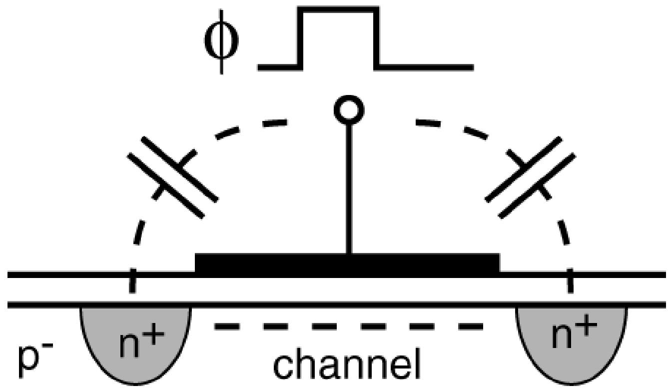
- reduced bandwidth
- increased circuit complexity
- aliasing & intermodulation issues

Auto-zero Principle



- S1,2 closed ⇒ amplifier offset is stored on C_{az}
- S3 closed ⇒ output signal is available
- Residual offset ~ V_{os}/A

Charge Injection (1)

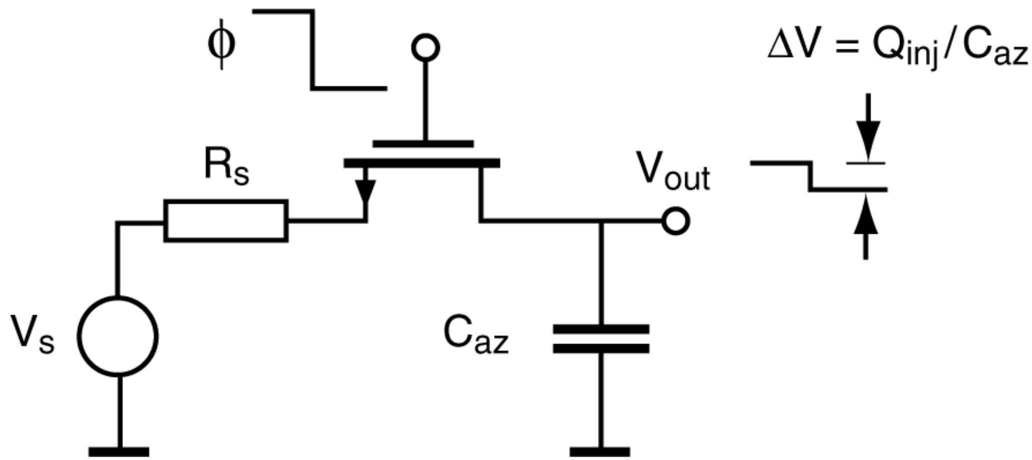


Occurs when MOSFETs switch **OFF**

Consists of two components

1. Channel charge, $Q_{ch} = WLC_{ox}(V_{GS}-V_t)$
2. Overlap capacitance between the gate and the source/drain diffusions

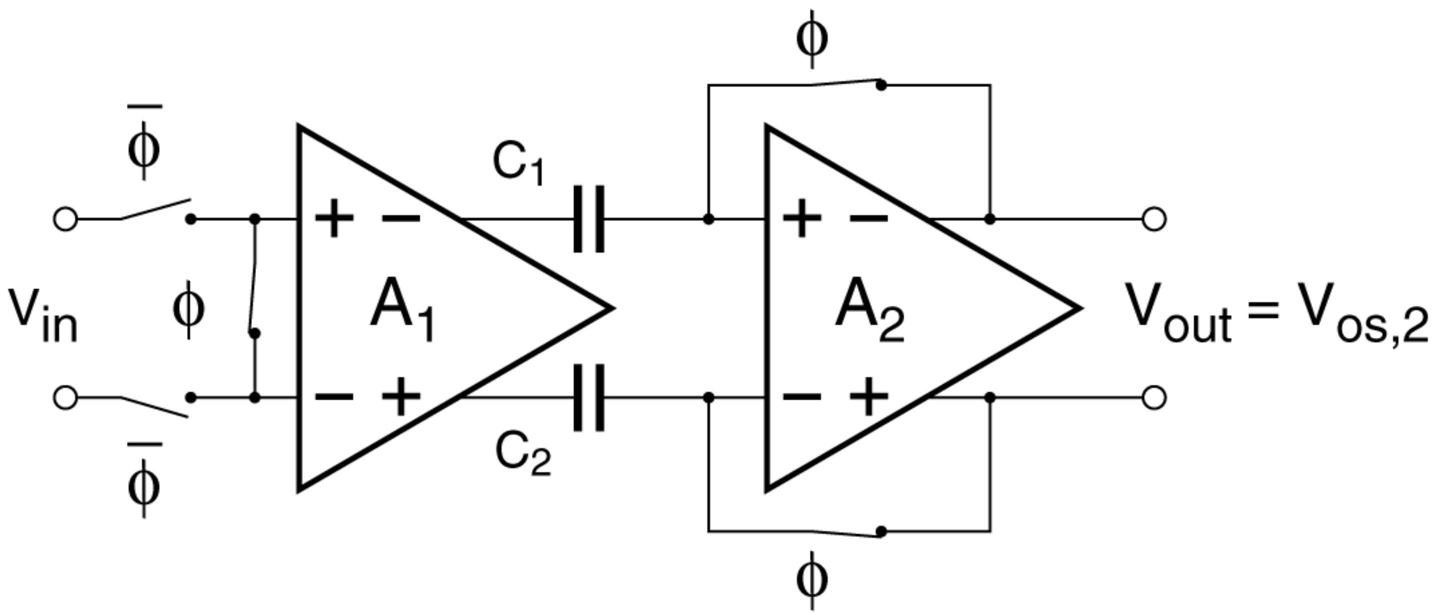
Charge Injection (2)



Error voltage depends on [4,5]

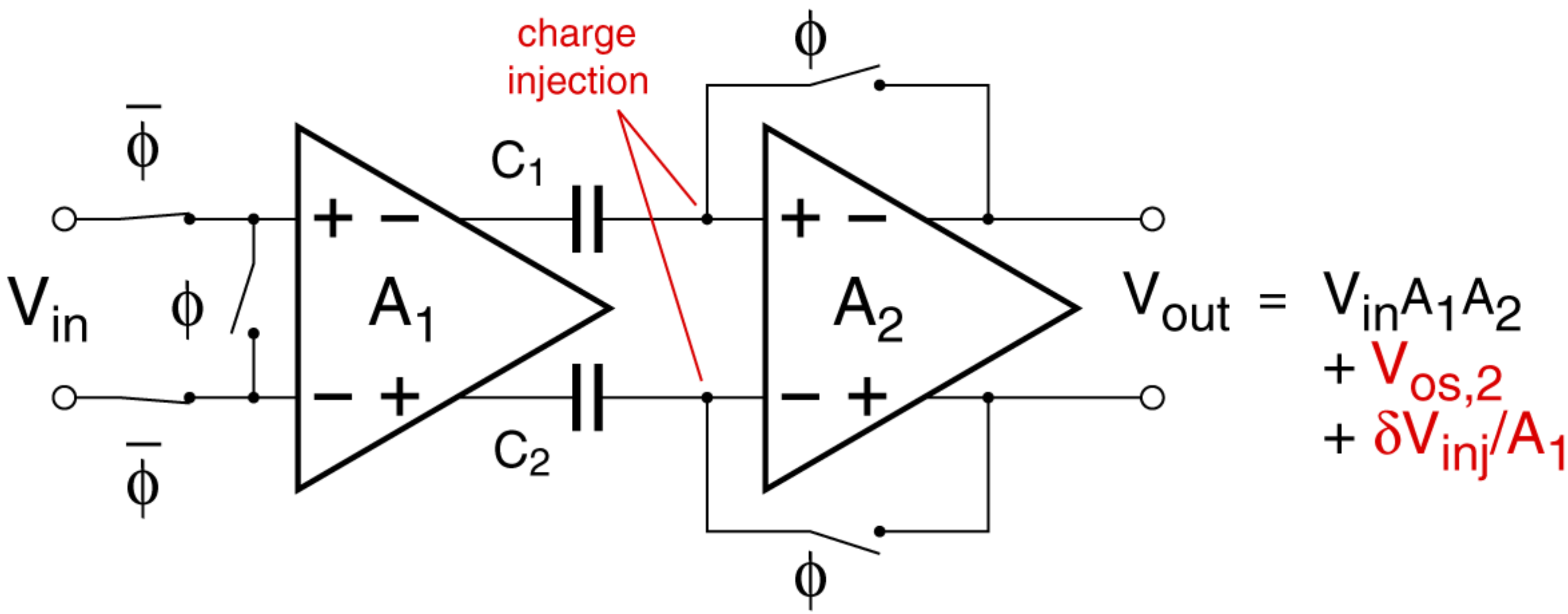
- Source impedance
- Transistor area (WL)
- Value of C_{az}
- Clock amplitude & slew rate

Switched Capacitor Amplifier (1)



- During the auto-zero phase, the offset of A_1 and A_2 is stored on $C_{1,2}$

Switched Capacitor Amplifier (2)



- During the next phase, V_{in} is amplified
- Differential topology $\Rightarrow$ 1st order cancellation of charge injection errors

Residual Offset of Auto-zeroing

Determined by

- Charge injection
- Leakage on C_{az}
- Limited amplifier gain & bandwidth (f_c)

In practice

- C_{az} as large as possible (sometimes external)
- Multi-stage amplifier topologies
- $f_c >> $ sampling frequency f_s
- Residual offsets of 1-10μV

Residual Noise of Auto-zeroing (1)

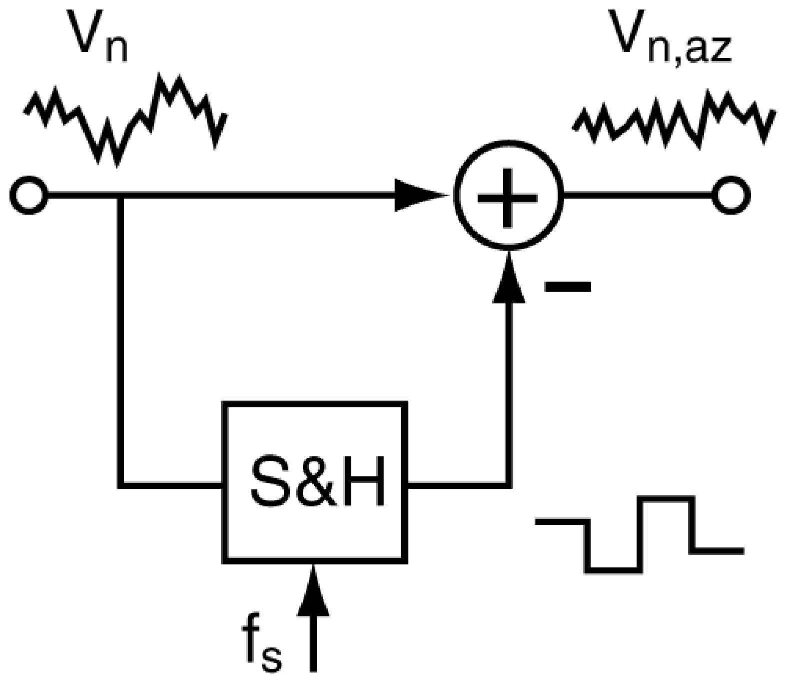
$V_{n,az}(f) = V_n(f)*(1 - H(f))$

H(f) is the frequency response of the S&H

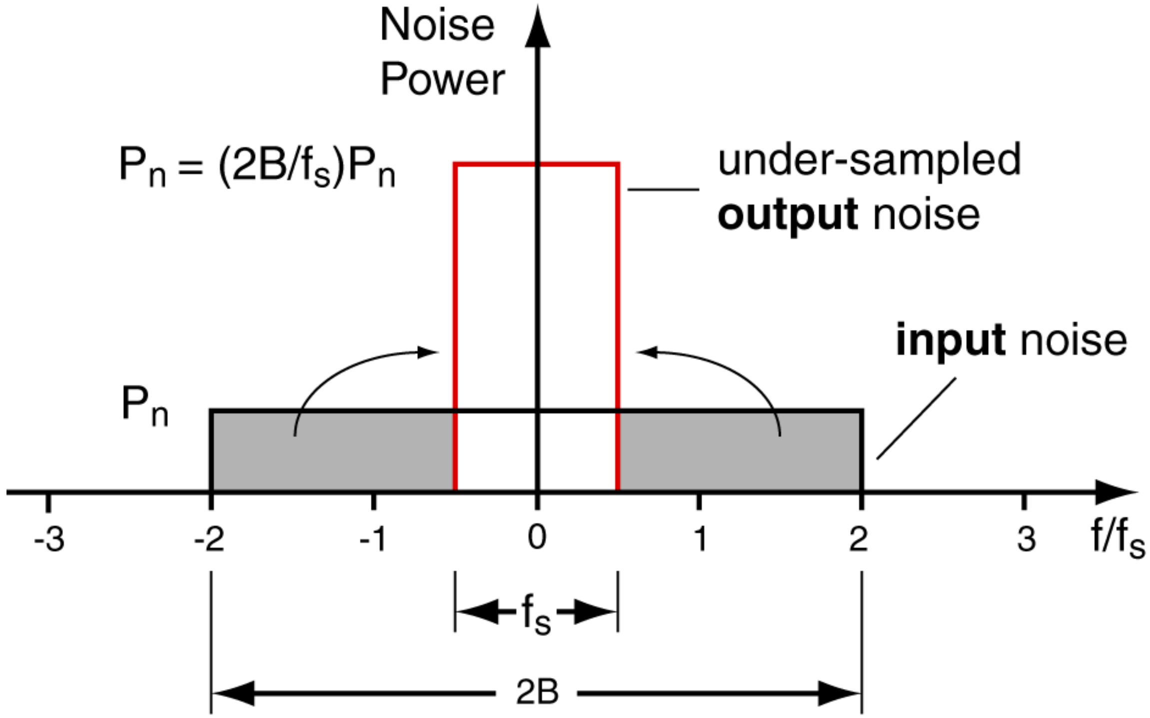
H(f) = sinc(f)

⇒ 1-H(f) is a HPF

⇒ Offset and 1/*f* noise reduction!

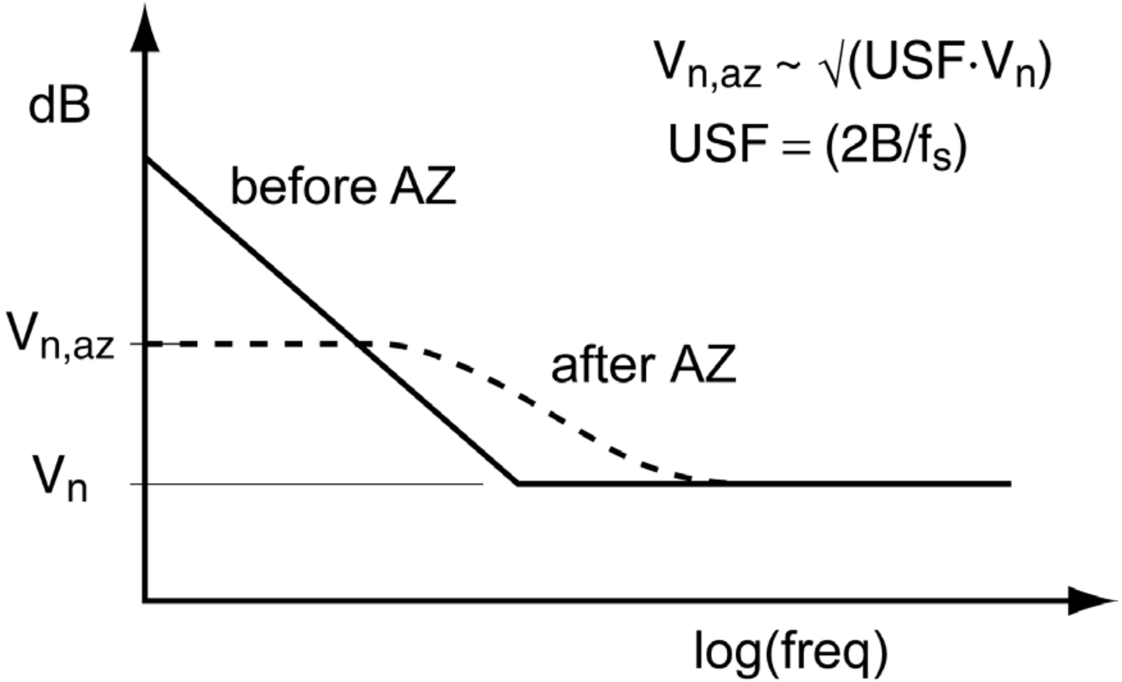


Residual Noise of Auto-zeroing (2)



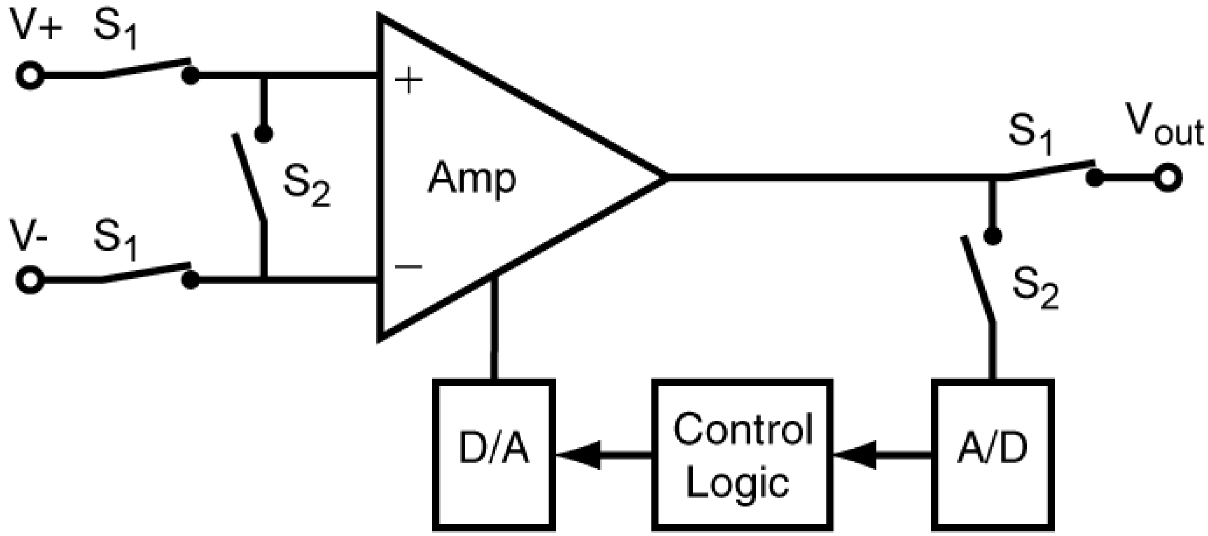
- Since noise bandwidth $B > f_s \Rightarrow$ input noise is folded back to DC
- The result is LP filtered by the Hold function

Residual Noise of Auto-zeroing (3)



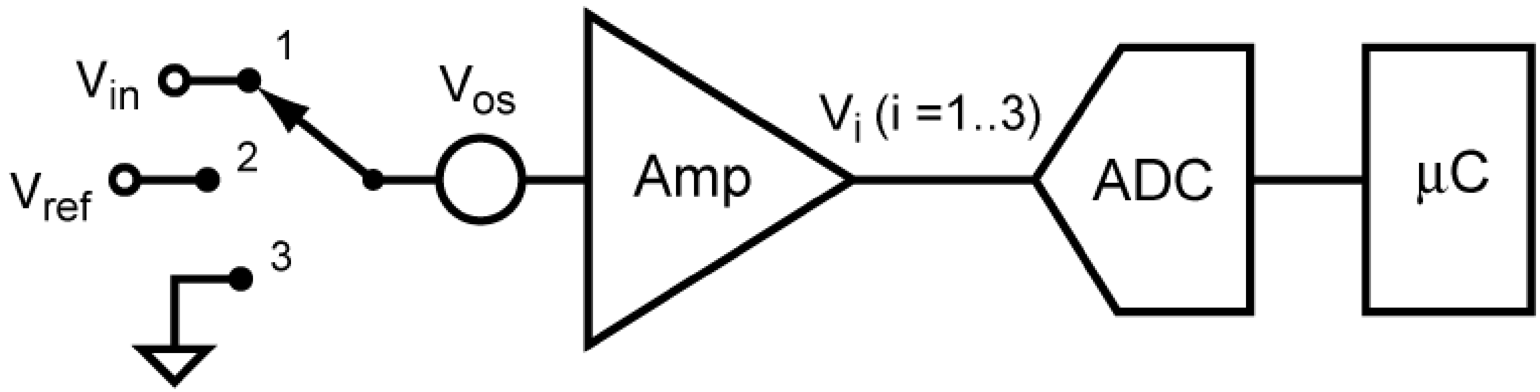
- 1/*f* noise is removed **but** noise foldover occurs [6]
- For a 1st order LPF, $B = \pi f_c/2$
- State of the art is 48nV/√Hz [7]

Digital Trimming



- Auto-zero at power on [8]
- No reduction of 1/*f* noise
- But no bandwidth limitation
- Residual offset determined by D/A resolution

The 3 Signal Method

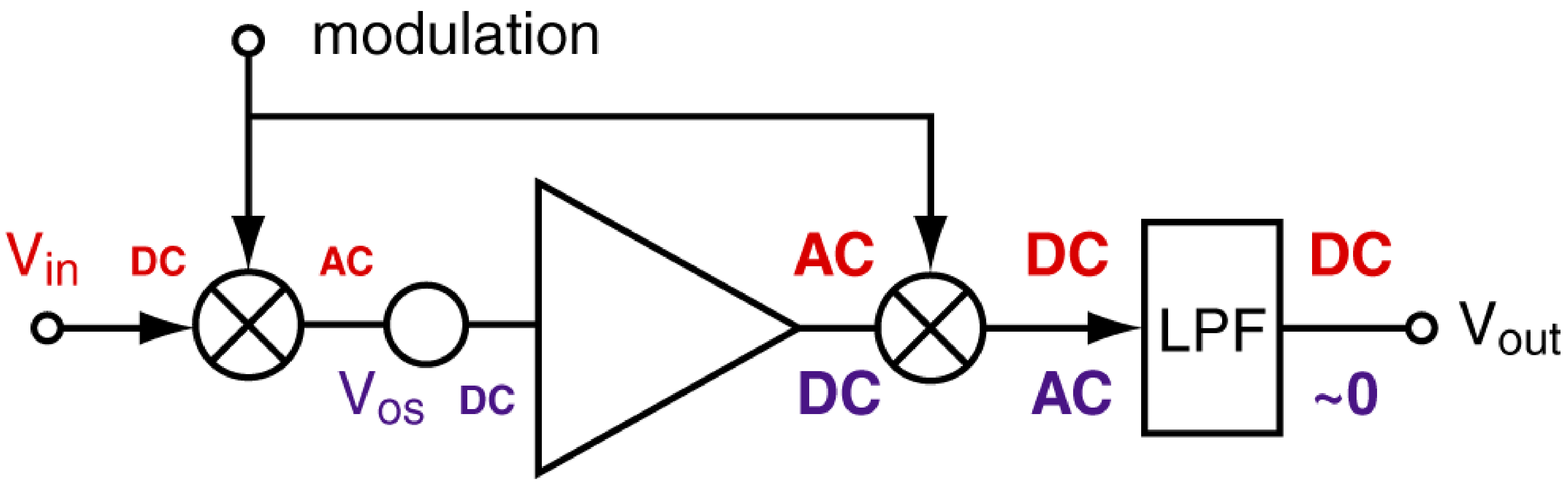


- Phase 1: $V_1 = A(V_{os} + V_{in})$
- Phase 2: $V_2 = A(V_{os} + V_{ref})$
- Phase 3: $V_3 = AV_{os}$

$\Rightarrow$ A,V_{os} and V_{in} can be calculated

- Easy to implement if a µC is available

Chopping Principle

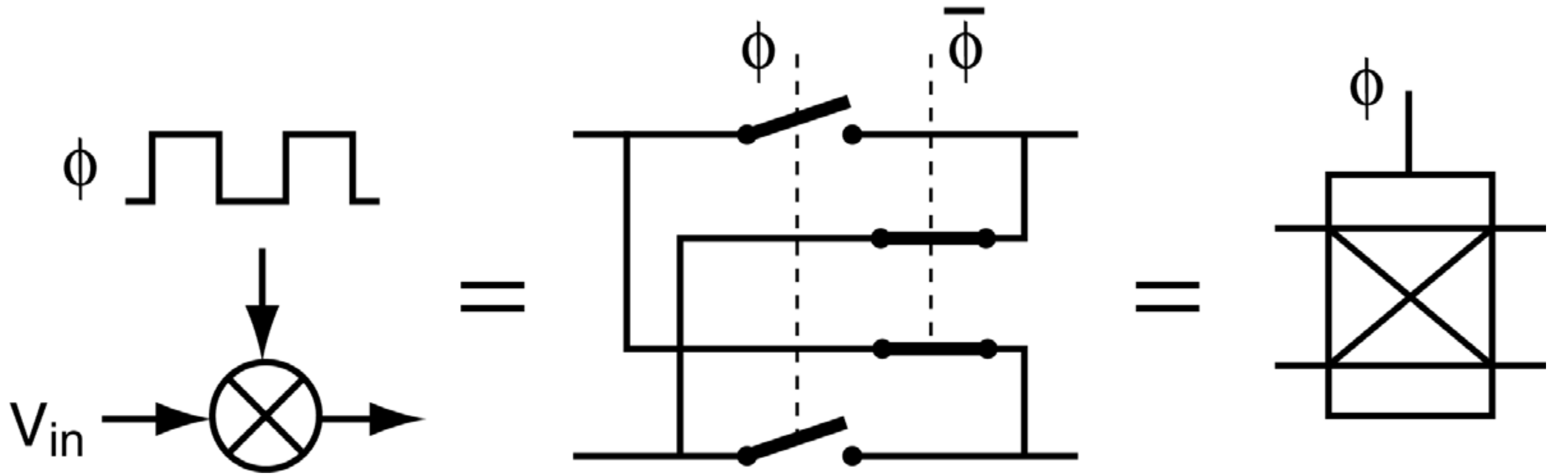


Signal is modulated, amplified and then demodulated again [9]

+ Output signal is continuously available

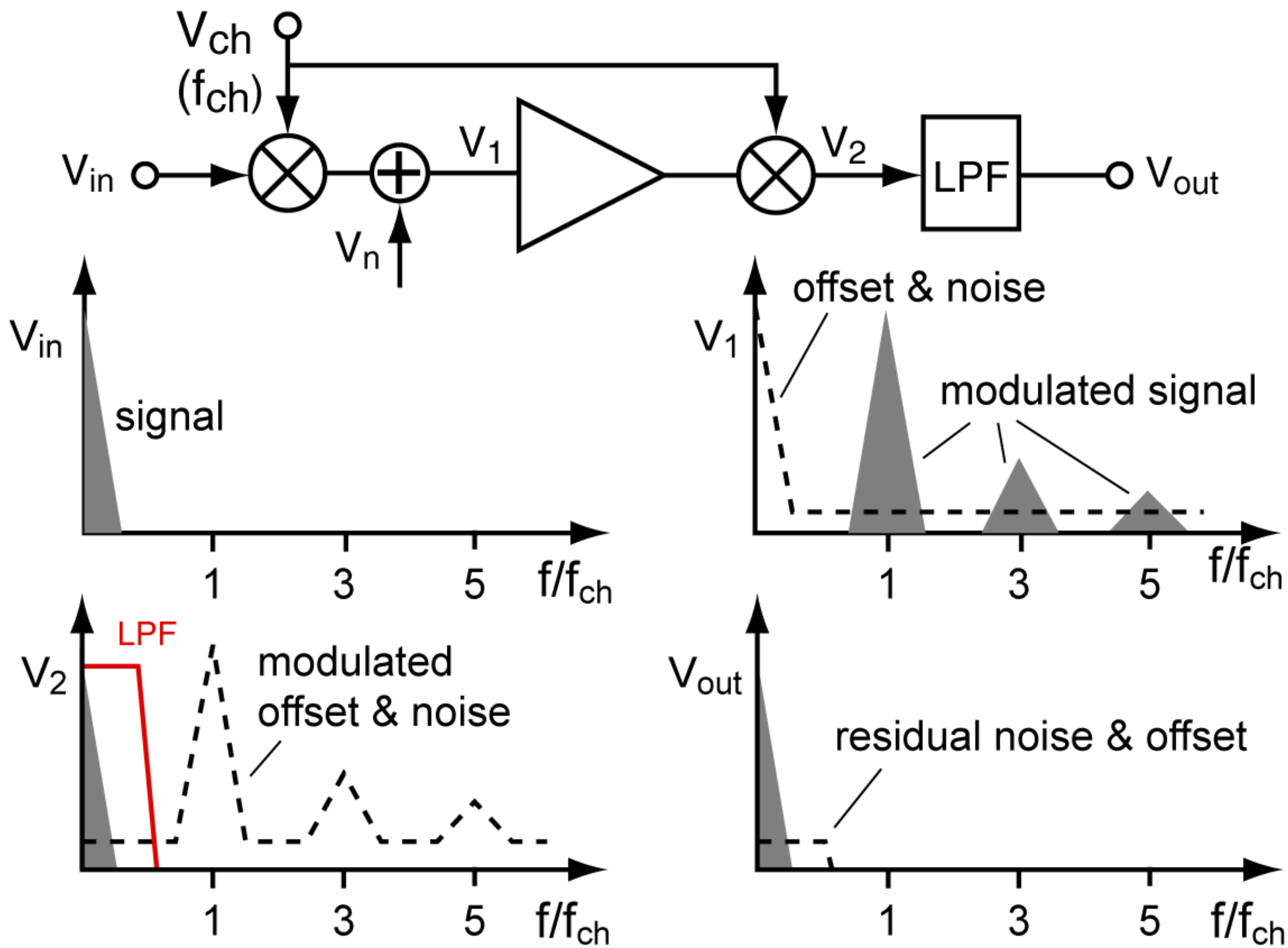
- Low-pass filter required

Square-wave Modulation

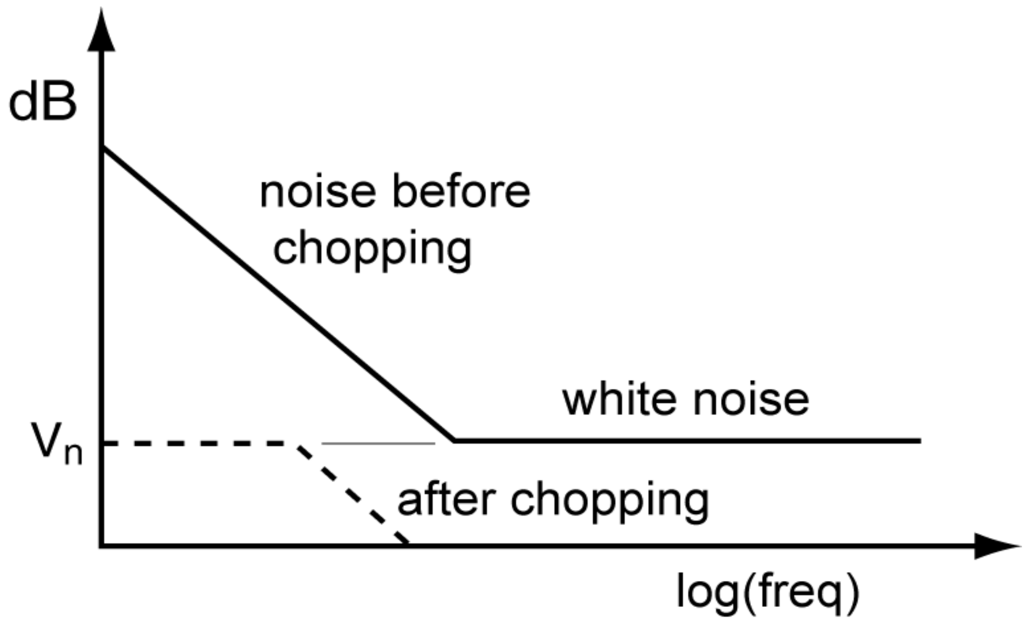


- Easily generated modulating signal
- The modulator is a polarity-reversing switch
- Switches are easily realized in CMOS

Chopping in the Frequency Domain

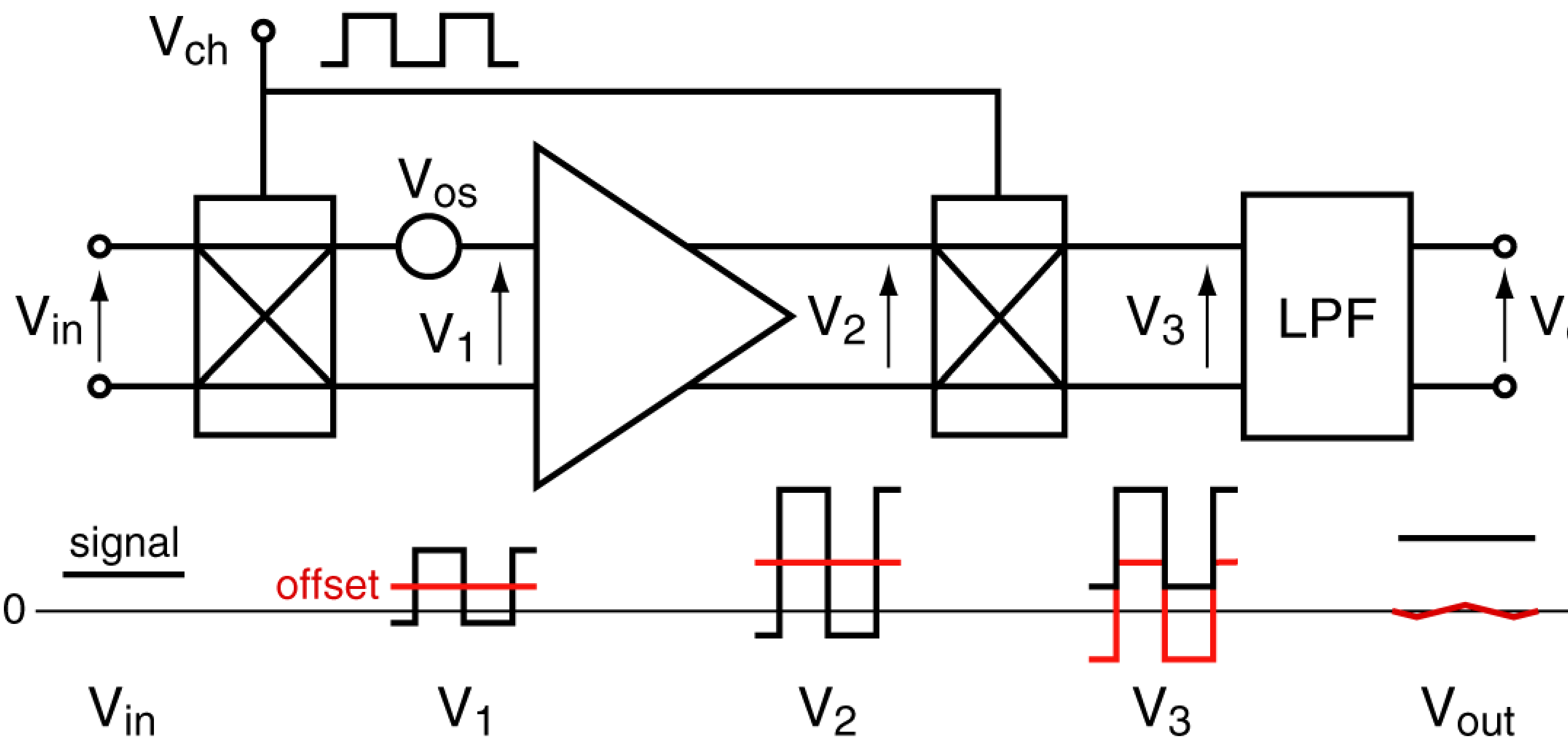


Residual Noise of Chopping



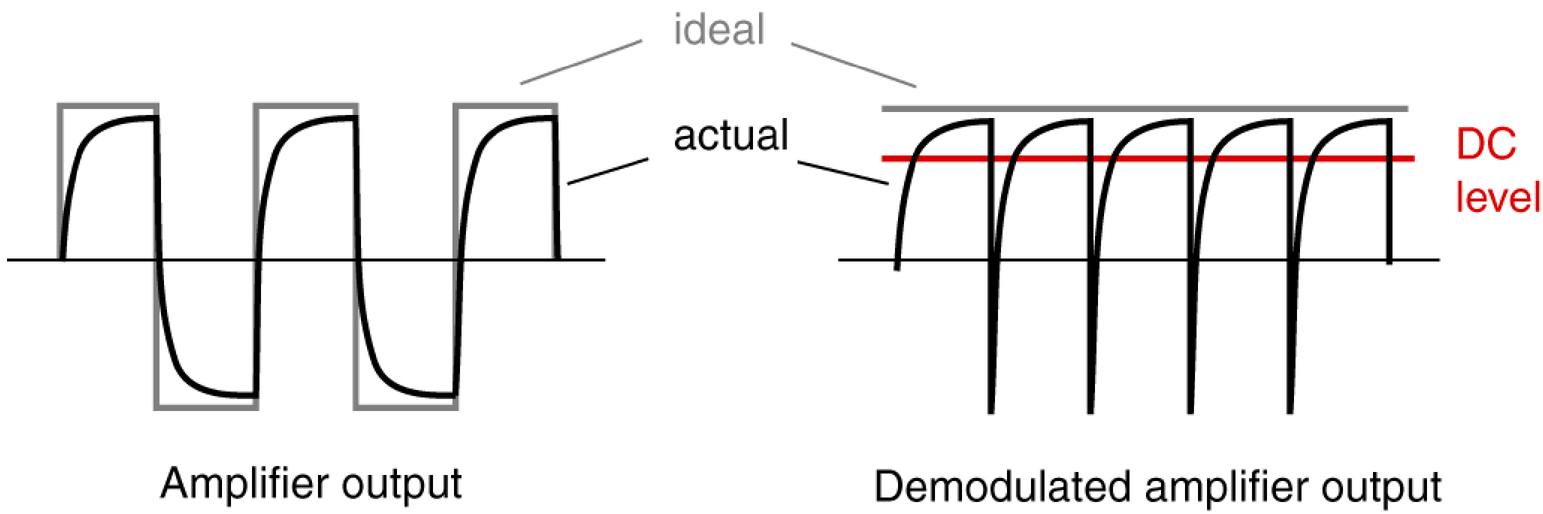
- 1/*f* noise is **completely** removed provided [6] f_{ch} > 1/f corner frequency
- Significantly better than auto-zeroing!
- State-of-the-art is 8.5nV/√Hz [10]

Chopping in the Time Domain



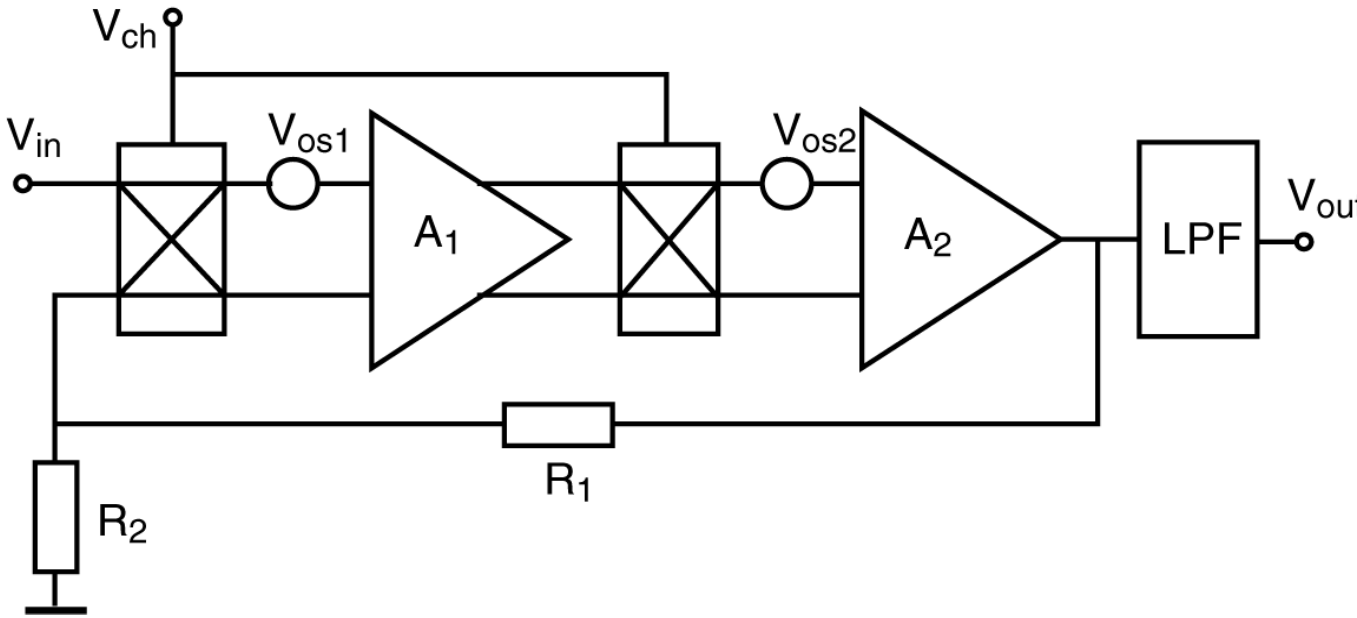
- Clock duty-cycle should be exactly 50% ⇒ ÷2

Bandwidth & Gain Accuracy



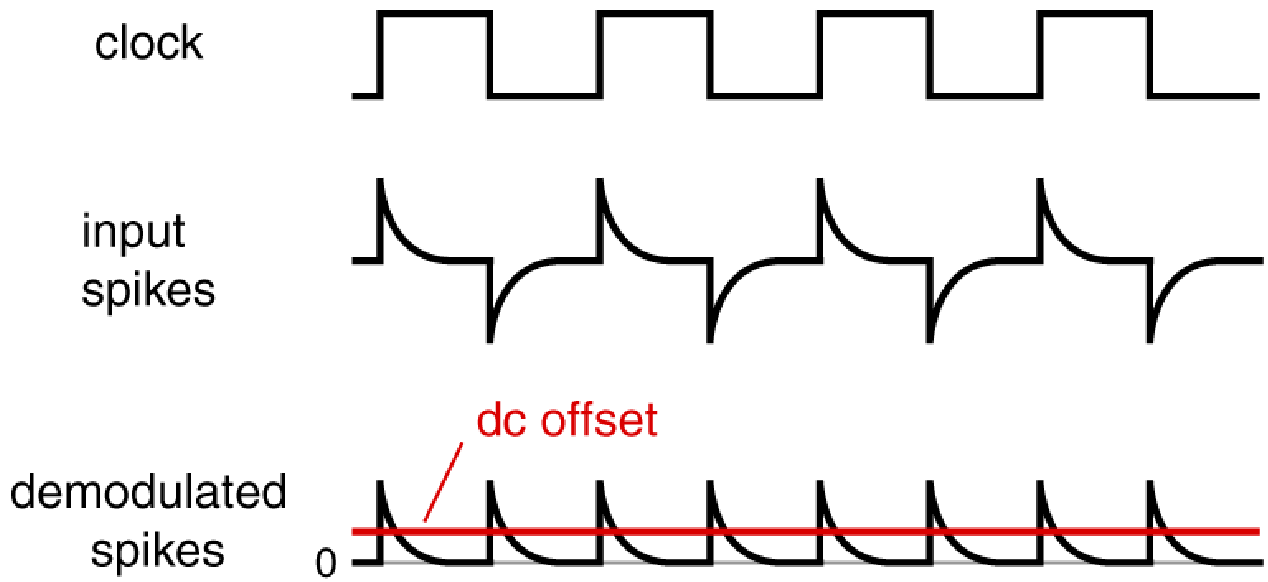
- Limited BW reduces effective gain
- $A_{eff} = A_{nom}(1\text{-}4\tau/T)$ for a 1st order LPF, where $f_{ch} = 1/(2\pi\tau)$ and $\tau << T$
- $T/\tau = 40 \Rightarrow 10\%$ error!

Chopper Opamp



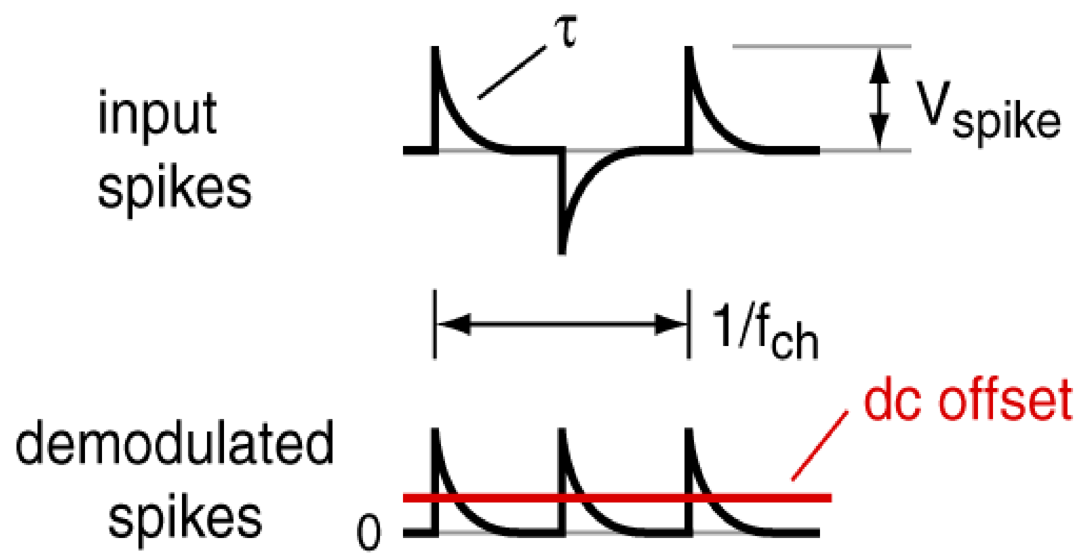
- Feedback resistors ⇒ Accurate gain [11,12]
- Offset is modulated, not the signal!
- To suppress V_{os2}, A_1 should have high gain

Residual Offset of Chopping (1)



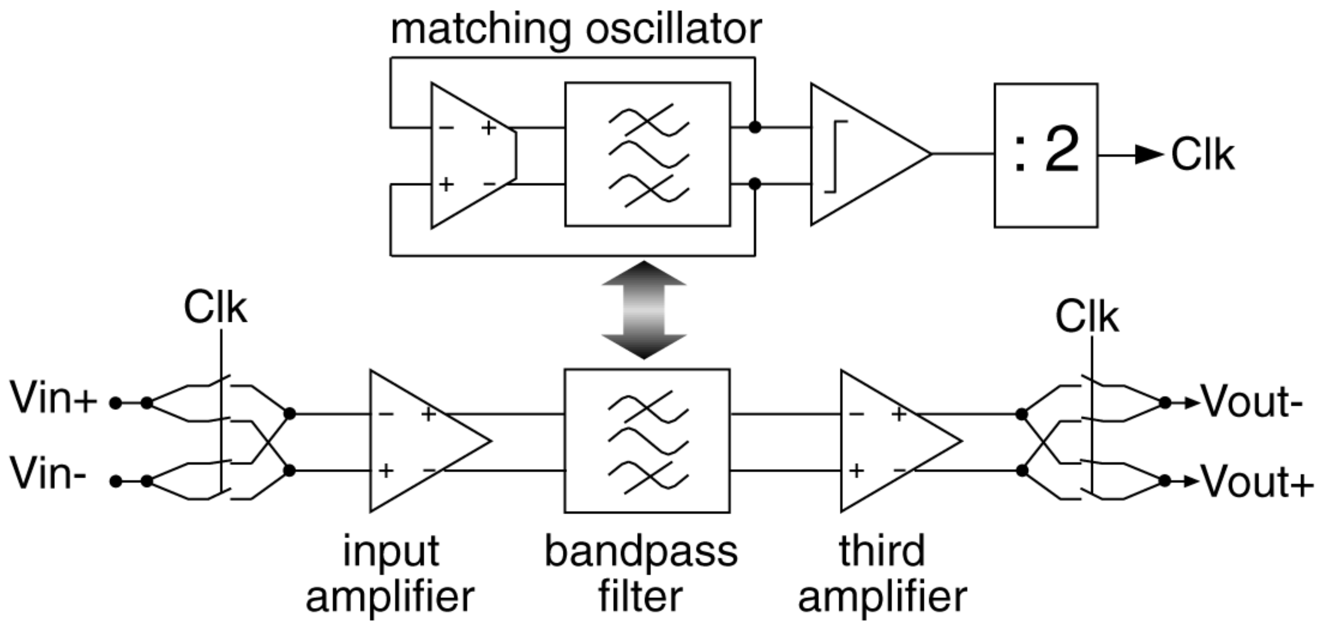
- Due to charge injection at the input chopper
- Causes a typical offset of a few μV
- Input spikes $\Rightarrow$ bias current (a few tens of pA)

Residual Offset of Chopping (2)



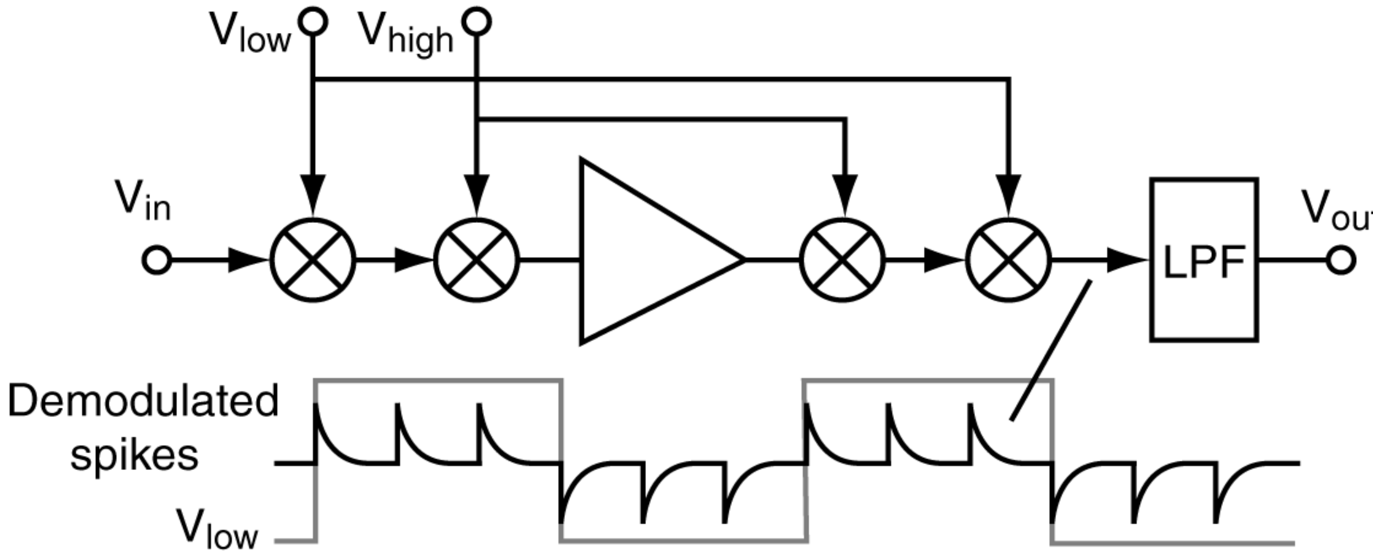
- Residual offset = $2f_{ch}\, V_{spike}\, \tau$
- Linearly dependent on chopping frequency f_s
- Spike time constant τ will vary with source impedance

Band-pass Filtering



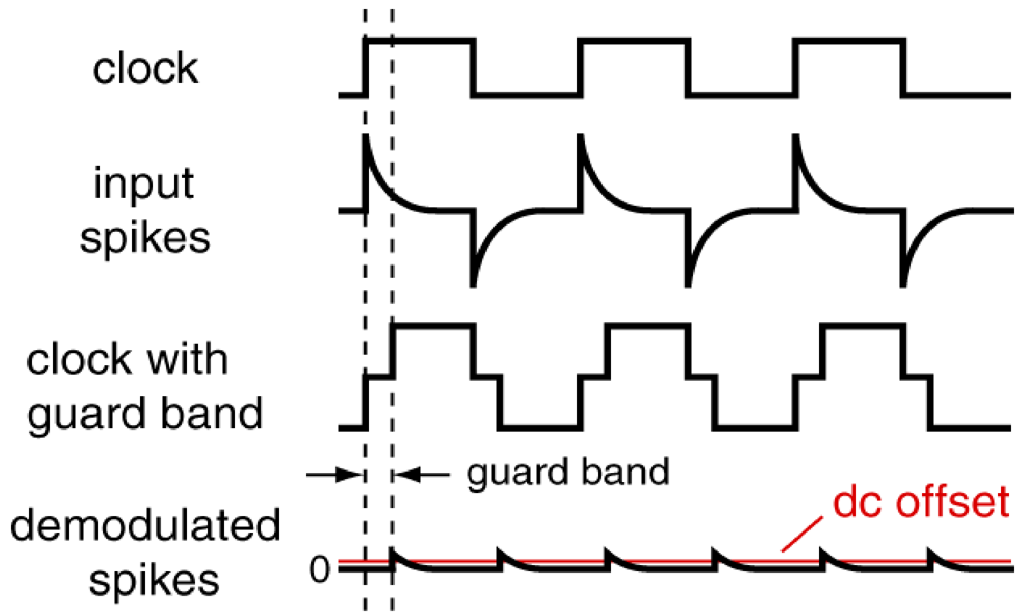
- BP (LP) filter reduces spike amplitude [10,13]
- Clock frequency tracks BP fillter's center frequency $\Rightarrow$ low filter Q ~ 5
- Residual offset < 1μV!

Nested Chopper



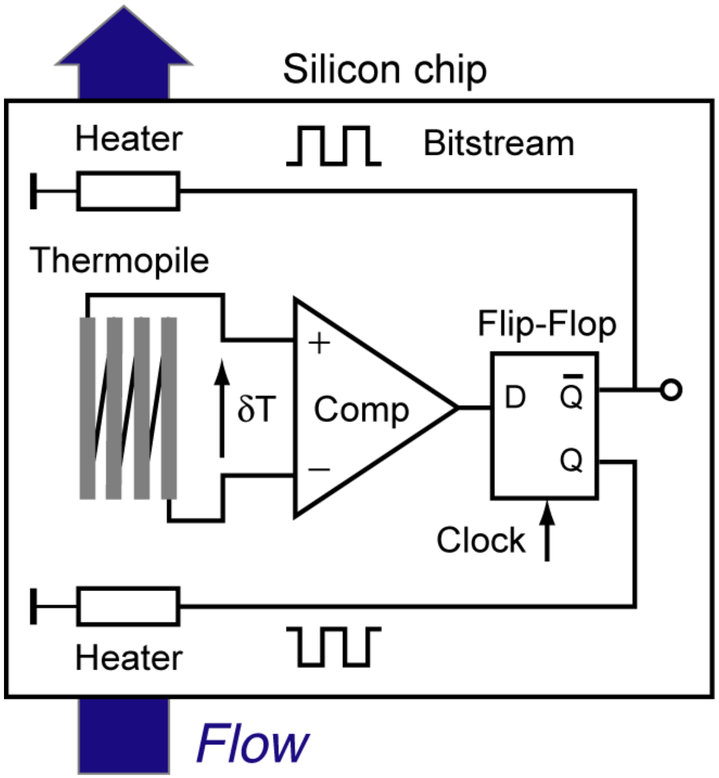
- Inner chopper removes 1/*f* noise
- Outer chopper removes residual offset [11,14]
- Residual offset ~ 100nV!

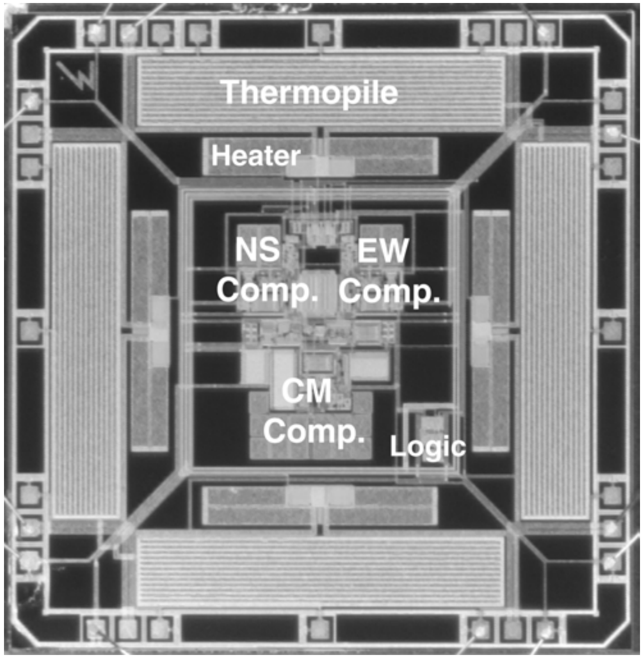
Chopper With Guard Band



- During guard-band, output is shorted [15,16] or tri-stated [17]
- Residual offset ~ 200nV!
- Slightly worse noise performance

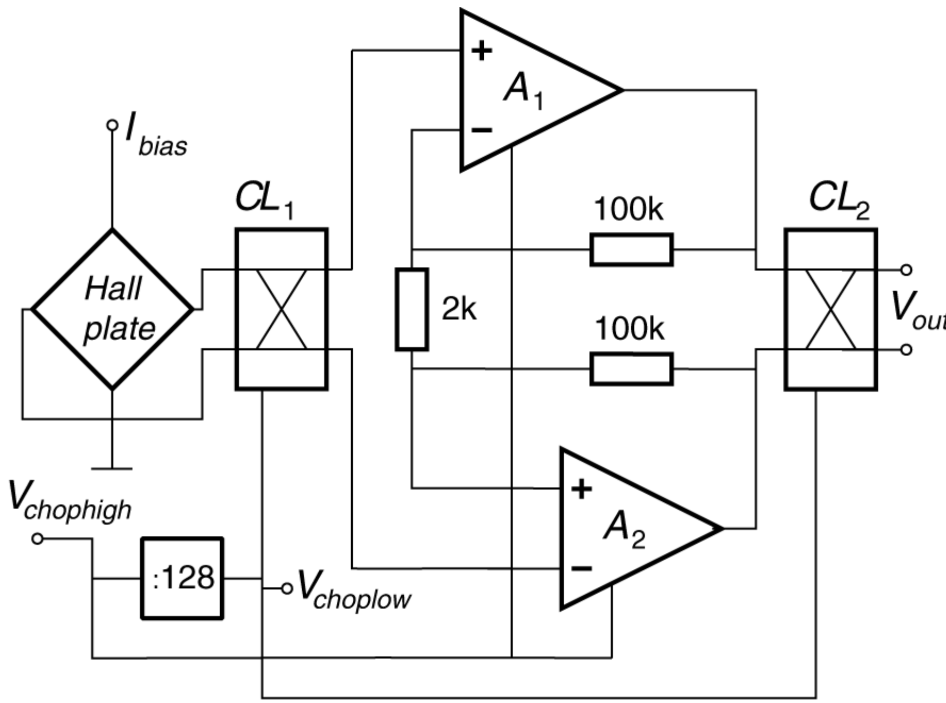
Smart Thermal Wind Sensor

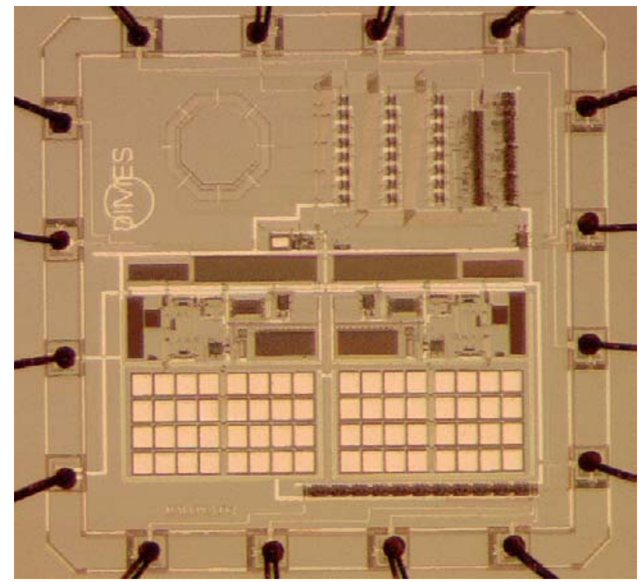




- Airflow induces a temperature gradient in chip
- Thermopiles are read-out by auto-zeroed comparators in a null-balance configuration [18]

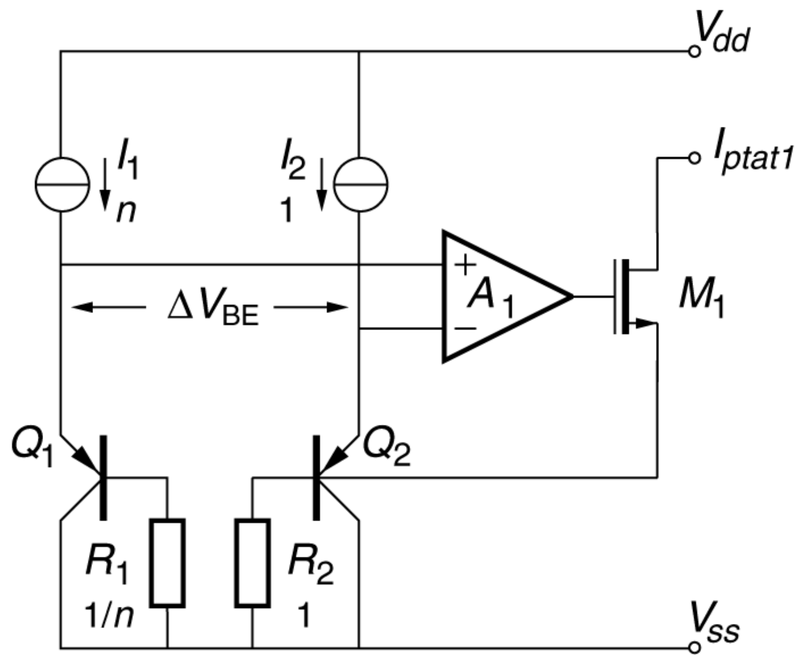
Smart Magnetic Field Sensor

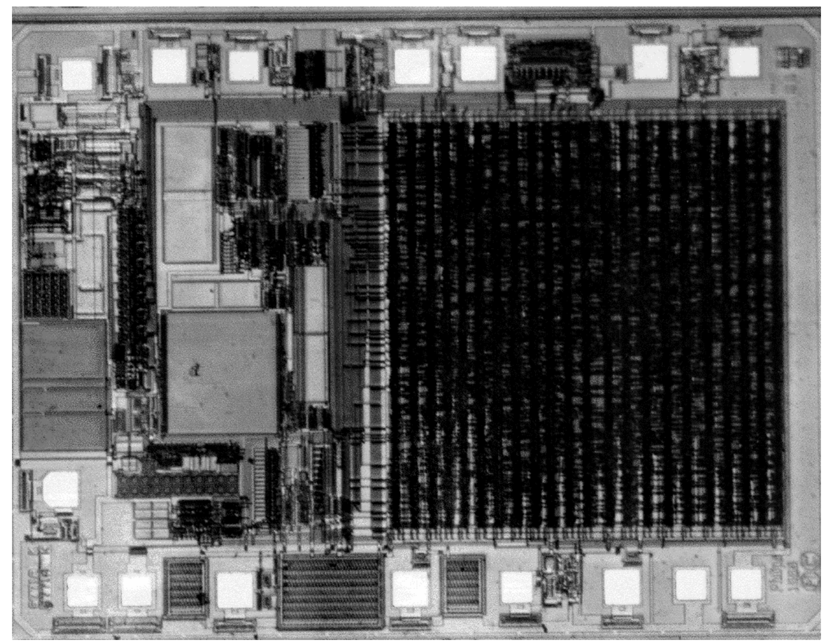




- Hall-plate is read-out using spinning-current & nested chopper techniques [19]
- Courtesy of A.Bakker, Philips Semiconductors, Delft

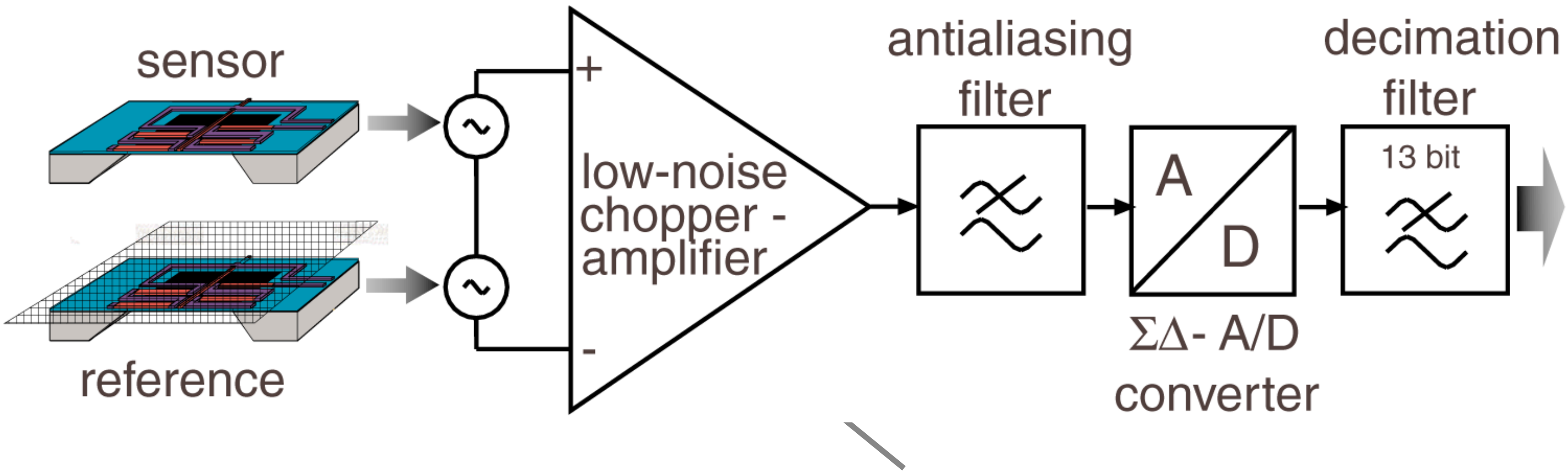
Smart Temperature Sensor

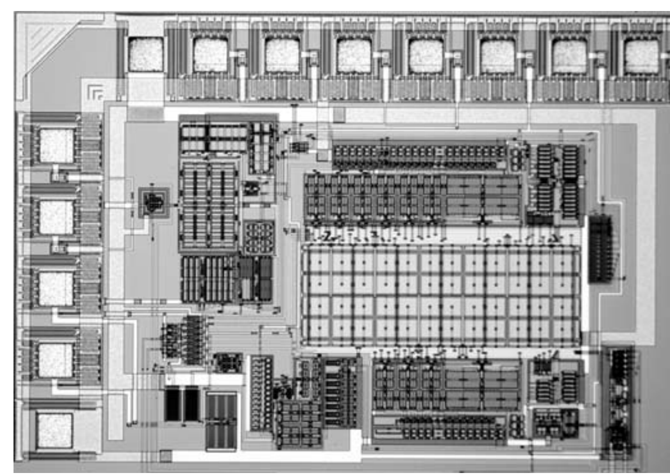




- ΔV_{be} ~ kT/q read-out using nested chopper technique $\Rightarrow$ ±1°C uncalibrated accuracy [14,20]
- Courtesy of A.Bakker, Philips Semiconductors, Delft

Smart Calorimetric Gas Sensor





- Calorimetric sensor read-out using BP chopper [21]
- Courtesy of C. Hagleitner, Physical Electronics Laboratory, ETH, Zurich

Summary

- Mismatch and offset are part of life
- Trimming reduces offset but not the noise
- Auto-zeroing only reduces LF noise, but does not limit amplifier bandwidth
- Chopping eliminates LF noise, but limits amplifier bandwidth

References (1)

1. P.R. Gray et al, “Analysis & Design of Analog Integrated Circuits,” 4th edition, John Wiley & Sons, Inc., 2000.
2. A. Hastings, “The Art of Analog Layout,” Prentice Hall, 2001.
3. G.A. Rincon-Mora, “Voltage references,” IEEE Press, 2002.
4. C. Eichenburger, W. Guggenbuhl, “On charge injection in analog MOS switches and dummy switch compensation techniques,” IEEE Trans. on Circuits & Systems, vol. 37, no. 2, Feb. 1990, p. 256-264.
5. C. Eichenberger, W. Guggenbuhl, “Charge injection of analogue CMOS switches,” IEE Proc. G: Circuits, Devices & Systems, vol. 138, no. 2, April 1991, p.155-159.
6. C.C. Enz, G.C.Temes, “Circuit techniques for reducing the effects of op-amp imperfections: autozeroing, correlated double sampling and chopper stabilization,” Proc. of the IEEE, vol. 84, no. 11, Nov. 1996, p. 1584 -1614.
7. Texas Instruments, TLC4501 data sheet, 1999.
8. Analog Devices Inc., AD8551 data sheet, 1999.

References (2)

9. C.C. Enz et al., “A CMOS chopper amplifier,” IEEE JSSC, vol.22, p.335-342, June 1987.
10. C. Menolfi, Q.Huang, “A fully integrated CMOS instrumentation amplifier with submicrovolt offset,” IEEE JSSC, vol. 34, March 1999, p.415-420.
11. A. Bakker et al., “A CMOS nested chopper instrumentation amplifier with 100nV offset,” IEEE JSSC, vol. 35, no. 12, 2000, p. 1877 - 1883.
12. K.A.A. Makinwa, J.H.Huijsing, “A wind sensor with an integrated low-offset instrumentation amplifier,” Proc. of ICECS 2001, vol. 3, p. 1505-1508.
13. C. Menolfi, Q. Huang, “A low-noise CMOS instrumentation amplifier for thermoelectric infrared detectors,” IEEE JSSC, vol. 32, no. 7, July 1997, p.968 - 976.
14. A. Bakker, “High-accuracy CMOS smart temperature sensors,” Kluwer Academic Publishers, Boston, 2000.
15. C. Menolfi, Q.Huang, “A 200nV 6.5 nV/√Hz noise PSD 5.6kHz chopper instrumentation amplifier,” Digest of ISSCC 2001, p. 362-363.

References (3)

16. A. Bilotti, G. Monreal, “Chopper-stabilized amplifiers with a track-and-hold signal demodulator,” IEEE Trans. On Circuits & Systems-I, vol. 46, April 1999, p. 490-495.
17. A. Thomsen, “DC measurement IC with 130nVpp noise in 10Hz, Digest of ISSCC 2000, p.334-335.
18. K.A.A. Makinwa, J.H.Huijsing, “A smart CMOS wind sensor,” Digest of ISSCC 2002, p.432-433.
19. A. Bakker, J.H.Huijsing, “Low-offset, low-noise 3.5mW CMOS spinning-current Hall-effect sensor with integrated chopper amplifier,” Proc. of Eurosensors XIII, Sept 1999, p.1045-1048.
20. C. Hagleitner et al., “N-well based CMOS calorimetric sensors,” Proc. of MEMS 2000, p. 96-101.